Value-Aware Scheduler for Energy Reduction

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***Abstract*—Optimizing energy consumption for computing workloads is a critical challenge, especially as we push the limits of high-performance systems within resource constraints. An underexplored approach to reducing energy costs is exploiting *value locality*: the tendency of instructions to process similar operand values during execution. Instruction operand values have abundant similarities within the reachable instruction window, a factor that existing architectures currently ignore. This paper introduces the broad concept of instruction-level, value-aware scheduling, an approach that leverages value locality in the hardware scheduler. By redirecting instructions of similar operand values to move together down the pipeline, the scheduler can reduce switching activity and dynamic energy usage. Such value-aware design philosophy, capable of adapting to a diverse range of workloads and architectures, has potential to be applied in broader architectural improvements.**

I. Introduction

Energy efficiency is a critical concern in modern computing [1]. While static energy usage remains relatively constant, dynamic energy usage is tied to the circuit switching activity (the number of bit flips) during program execution and presents opportunities for optimization. By executing programs in a manner that reduces switching activity, we can save dynamic energy without affecting the result and the performance of the program.

One promising program feature that can be leveraged for energy reduction is value locality. Value locality refers to similar instruction operand values occurring throughout the program. Since register transitions between similar values can lead to lesser switching activity compared to transitions between uncorrelated values, we can reduce dynamic energy consumption if we are operating on similar, **consecutive** values on the same data path.

Prior research has shown a high degree of operand value similarities observed at the hardware architecture level [2] [3]. However, most existing exploitations on value locality require either compiler support [4] [5] or fine-tuning in the program [3] [6]. Few have directly exploited this knowledge for dynamic optimization in hardware. This paper introduces the concept of **value-aware hardware scheduling** that can reduce energy consumption by scheduling instructions with similar operand values together, as illustrated in Figure 1. While state-of-the-art schedulers assign an instruction onto the first execution lane available, a value-aware scheduler strategically assigns instructions with similar operands to flow down the pipeline consecutively. This scheduling policy minimizes switching activities between instructions and can reduce dynamic energy without changing the program.

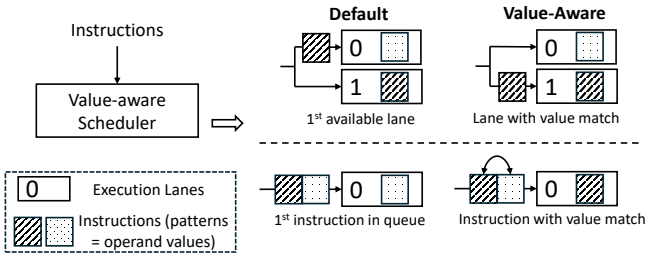


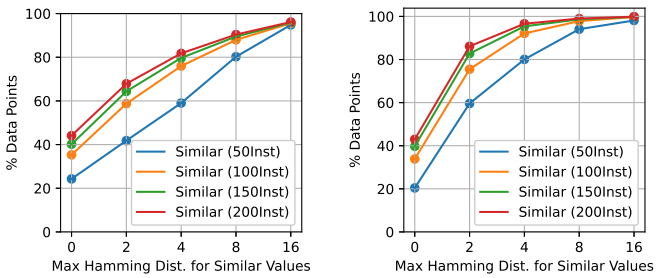
Fig. 1: Overall workflow for the proposed scheduling technique: a dynamic hardware scheduler that predicts instruction operand value similarities, and executes instructions with similar values consecutively on the same execution lane to reduce toggling.

II. Opportunities in Value Locality

Value locality can be classified into two types: **static value locality**, where one or a few values occur most of the time [2]; and **dynamic value locality**, where a value keeps changing but remains the same as the one generated elsewhere in the program [3]. Static value locality consists of values from constant sources or program regularities that are known at compile time [7] [8]. Dynamic value locality refers to variants coming from program inputs that vary from run to run and can only be known at runtime [3] [9] [10]. Although the program input is typically different across program runs, there is usually a consistent pattern of similarity between data inputs [6]. For example, edge applications [11] [12] and big data applications [13] [14] process data from real-world which are naturally correlated. The proposed scheduling technique has the potential to optimize both dynamic and static locality to get the benefits of both worlds.

Figure 2 shows value locality in common applications, including SPEC2017 [15][1], a general-purpose benchmark suite, and EdgeBench [16], a data-intensive edge application benchmark suite (averaged across all individual benchmarks). For each testbench, we ran a trace of 100k instructions after the warmup stage (skipping first one billion instructions) and counted the number of non-memory instructions that have the

[1]These SPEC 2017 results are non-compliant estimates.



(a) SPEC2017 (General Purpose). (b) EdgeBench (Data Intensive).

Fig. 2: Percentage of non-memory instructions that have the first source operand value match with at least one other instruction within various instruction window lengths. Both benchmark suites show significant value locality; EdgeBench shows more data input similarities while SPEC2017 shows more program-related value correlation.

first source operand value match with at least one other instruction within specific instruction window lengths. The degree of similarity between operand values further increases when we relax the constraint of exact matches to approximate matches, with the number of bit differences (Hamming Distance [17]) as the distance metric. In order to study value similarity, we used Intel Pin [18] to generate single-thread traces annotated with each instruction's source operand values, and pass them into a self-developed Python post-processor to find values that are similar with those in nearby instructions.

While both benchmark suites show value locality from program-related and input-related patterns, EdgeBench shows more commonality among inherently correlated data inputs compared to SPEC2017, which increases the percentage of value locality for small but non-zero hamming distances. If the microarchitecture can locate these similar values, it can effectively decrease bit-level switching activities on critical datapaths including ALUs and downstream execution units.

III. Implementation Insights

A. Predicting Value Locality

An ideal value-aware scheduler would know the source operand values of instructions before making lane assignments, but obtaining these values is impractical. Although operand values are available in the pipeline when the instruction is ready to be issued, accessing them either requires additional reads from the register file or complex logic for reading from bypassing. Both of these alternatives add complexity and require extra pipeline stages on the critical path. Scheduling decisions need to be done by **predicting operand correlations before knowing the actual values**. To avoid adding latency, the prediction can be done **off the critical path** between the fetch and the issue stage, based on the instruction's PC that is available at the fetch stage.

B. Targeting Instructions

The proposed scheduler can focus on rescheduling *ready-to-execute* instructions. Ready-to-execute instructions are those with no unresolved dependencies, and can be issued immediately if an execution lane is available. The concepts for the scheduler can be applied to both non-memory and memory instructions. While non-memory instructions are more intuitive, reordering memory instructions requires meticulous management for memory dependencies.

C. Maintaining Original Performance

To preserve original performance of the application, the scheduler could be made to only reassign instructions launched in the same cycle to difference execution lanes for better value matches. While this approach can bring decent energy reduction, we can further reorder instructions in different cycles to exploit value locality beyond neighboring cycles with minimal performance impact. However, for instructions without immediate value correlation matches, indefinitely delaying issuing to wait for future matches might lead to performance drop. The impact is serious if the instructions on the critical path are being pushed back when there is no value match. To preserve original performance, we need to prioritize issuing instructions on the critical path.

IV. Broader Implications

The principles for designing value-aware schedulers can be applied to value locality on other granularity levels, other hardware platforms, and diverse scenarios for architectural improvements. Exploring the unique value locality characteristics of specialized operand types, such as Intel's X86-64 architecture's Vector operands, or specific instructions types, can lead to fine-tuning for different operands or instructions for energy reduction. The scheduling strategy can also be applied to architectures beyond the CPU we modeled. The approach is feasible for any system with flexible instruction issuing.

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